

ISO 9001:2015 AICTE-CII: GOLD Category Institute NAAC-'A' Grade Institute (CGPA: 3.21) NIRF-2020 Rank Band: 201-250

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE
 Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.
 काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत
 కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫ తెలంగాణ, భారతదేశము
 (An Autonomous Institute under Kakatiya University, Warangal)
 (Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech. CLASSWORK TIME TABLE for the EVEN SEMESTER of Academic Year 2022-23

II SEMESTER of M.Tech (ES & VLSI)

ClassTeacher : Dr. B. Jeevan

w.e.f 12.06.2023

Day	08.00-08.50 am	08.50-09.40 am	09.40 -10.30 am	B R E A K	10.50-11.40 am	11.40 am-12.30 pm	12:30-01:20pm
Mon	LVLSI	AICD	DM		←----- AICD Lab (EV_M.TECH_II SEM) GR --→		
Tue	ESDWRTOS	ASCD	DM		←----- ASCD Lab --→ (EV_M.TECH_II SEM) MQ		
Wed	←----- ASCD Lab --→ (EV_M.TECH_II SEM) MQ				ASCD	LVLSI	LIBRARY
Thu	ASCD	ESDWRTOS	AICD		←----- AICD Lab--→ (EV_M.TECH_II SEM) GR		
Fri	AICD	←-----MINI PROJECT---→			LVLSI	ESDWRTOS	LIBRARY
Sat	-	-	-		-	-	-

CourseTitle	CourseCode&CourseName	CourseFaculty
AICD	: P20EV201: Analog IC Design	: Sri G. Raju (GR)
ASCD	: P20EV202:Advanced System On Chip Design	: Abdul Muqeem(MQ)
LVLSI	: P20EV203A: Low Power VLSI Design	: Dr. B. Jeevan (BJ)
ESDWRTOS	: P20EV204A: Embedded Systems Design with RTOS	: Smt. K.Shailaja(KSJ)
DM	: P20AC208D: Disaster Management	: Sri S. Ashok(SA)
AICD Lab	: P20EV205: Analog IC Design Laboratory	: Sri G. Raju (GR)
ASCD Lab	: P20EV206: Advanced System On Chip Design Laboratory	: Abdul Muqeem(MQ)
Mini Project	P20EV207 : Mini Project with Seminar	

Sd/-
Faculty I/c,
Dept.Timetables

Sd/-
Faculty I/c, Overall
Timetables

Sd/-
Programme Head,
ECI

Sd/-
HoD, ECE

Sd/-
Dean, AA

Sd/-
Principal